Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-68 (canceled)

69. (currently amended) A semiconductor chip with a wirebonded wire, comprising:

a silicon substrate;

an active device in and on said silicon substrate;

a first dielectric layer over said silicon substrate;

an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region;

a second dielectric layer between said first and second metal layers;

a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region ~~and exposes said first region~~;

an aluminum cap comprising a first portion directly over said first region and a second portion directly over said passivation layer, wherein said aluminum cap is connected to said copper pad through said opening in said passivation layer, and wherein said aluminum cap has a width greater than that of said opening in said passivation layer;

an adhesion/barrier layer on said aluminum cap; and

a gold layer on said adhesion/barrier layer and directly over said first and second portions of said aluminum cap, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said electroplated gold layer has a thickness between 2 and 20 micrometers, and wherein said wirebonded wire is joined with said gold layer.

70. (previously presented) The semiconductor chip of claim 69, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip.

71. (previously presented) The semiconductor chip of claim 69, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip.

72. (previously presented) The semiconductor chip of claim 69, wherein said adhesion/barrier layer comprises tantalum.

73. (previously presented) The semiconductor chip of claim 69 further comprising a polymer layer between said adhesion/barrier layer and said passivation layer, wherein said polymer layer has a thickness between 2 and 20 micrometers.

74. (previously presented) The semiconductor chip of claim 73, wherein said polymer layer comprises polyimide.

75. (previously presented) The semiconductor chip of claim 69 further comprising a third dielectric layer on said gold layer, wherein an opening in said third dielectric layer is over said gold layer joined with said wirebonded wire.

76. (previously presented) The semiconductor chip of claim 69, wherein said gold layer joined with said wirebonded wire is directly over said active device.

Claim 77 (canceled)

78. (previously presented) The semiconductor chip of claim 69, wherein said adhesion/barrier layer comprises titanium.

79. (previously presented) The semiconductor chip of claim 69, wherein said active device comprises a transistor.

80. (currently amended) A semiconductor chip with a wirebonded wire, comprising:

a silicon substrate;

an active device in and on said silicon substrate;

a first dielectric layer over said silicon substrate;

an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region;

a second dielectric layer between said first and second metal layers;

a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region ~~and exposes said first region~~;

an adhesion/barrier layer over said first region and over said passivation layer; ~~silicon substrate;~~ and

a gold layer on said adhesion/barrier layer, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer, and wherein said wirebonded wire is joined with said gold layer.

81. (previously presented) The semiconductor chip of claim 80, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip.

82. (previously presented) The semiconductor chip of claim 80, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip.

83. (previously presented) The semiconductor chip of claim 80, wherein said adhesion/barrier layer comprises tantalum.

84. (previously presented) The semiconductor chip of claim 80 further comprising a polymer layer between said adhesion/barrier layer and said passivation layer, wherein said polymer layer has a thickness between 2 and 20 micrometers.

85. (previously presented) The semiconductor chip of claim 84, wherein said polymer layer comprises polyimide.

86. (previously presented) The semiconductor chip of claim 80 further comprising a third dielectric layer on said gold layer, wherein an opening in said third dielectric layer is over said gold layer joined with said wirebonded wire.

87. (previously presented) The semiconductor chip of claim 80, wherein said gold layer joined with said wirebonded wire is directly over said active device.

88. (previously presented) The semiconductor chip of claim 80, wherein said electroplated gold layer has a thickness between 2 and 20 micrometers.

89. (previously presented) The semiconductor chip of claim 80, wherein said adhesion/barrier layer comprises titanium.

90. (previously presented) The semiconductor chip of claim 80, wherein said active device comprises a transistor.